Standardizing an Increasingly 3D World

Sitaram Arkalgud
SEMATECH

Introduction

Stacking chips and connecting them with through silicon vias (TSVs) offers the benefits of less power consumption, better performance, greater density, smaller footprint/package size and lower cost.[1] Although the concept has been proposed for several decades,[2,3] the cost of fabricating 2D chips has always been lower than 3D chip stacks. However, given the growing complexity of fabricating chips at increasingly aggressive technology nodes, the cost of 3D stacking with TSVs appears attractive. In addition, TSVs offer a pathway to greater functionality while avoiding the complexity and cost structure of today's system-on-chip (SoC) solutions.

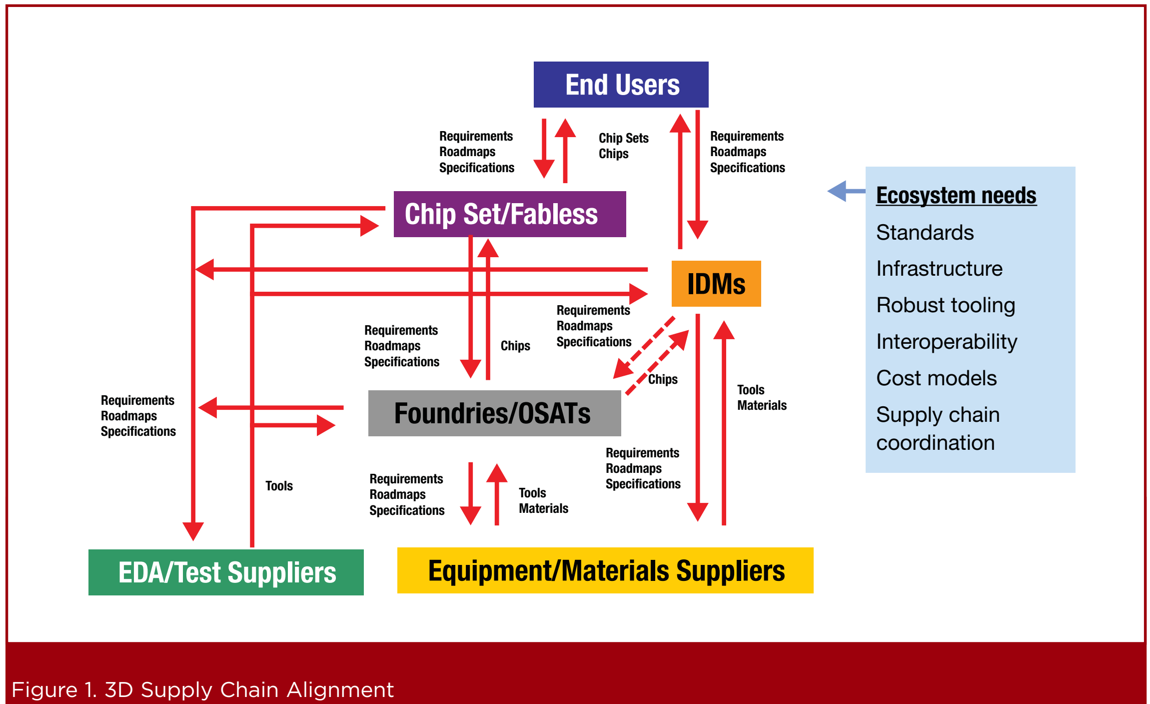

Figure 1. 3D Supply Chain Alignment

Factors Driving Standardization

To gain universal acceptance and be manufactured in high volumes, 3D needs to be standardized at several levels, largely because the semiconductor manufacturing landscape has changed considerably over the last two decades. Companies that once used to control their entire supply chain from manufacturing silicon wafers to final assembly and test are now specializing in core technologies and have divested the non-core areas, the result of which is an extremely fragmented ecosystem, as shown in Figure 1. While the ecosystem has been optimized for a 2D world, 3D technology could shift traditional roles from one area in the industry to another, and obscure the expected value-add from each participant. Credible, standardized reference flows can address this issue and ensure that infrastructure needs, such as robust tooling, interoperability, cost models and supply chain coordination, work together to deliver cost-effective solutions.

Technical Area		Driver	Stds Body	
D2D Layout compatibility	Bump Layout			Single bump size and shape
	Bump Array Layout	Die Supplier	JEDEC	Array size and shape
	Bump Assignment			e.g., specialized locations for DFT
PDK Modeling compatibility	Electrical Model Format	SEMATECH		How to manage coupling and stuff
	Thermal Model Format	& GSA	Si2	Material properties, char. & validation methods
	Stress Model Format	SEMATECH W/S		Material properties, characterization methods
Design design database compatibility	PF Exchange Formats	imec		Partitioning info, floor planning info
	Stress Exchange Formats	EDA		I/P for stress sim + O/P stress map
	Temp Exchange Formats	EDA	Si2	I/P power map + O/P temp map for timing
	PDN Exchange Format	EDA		Reduced order compact power model
	SI Exchange Format	EDA		Equivalent of IBIS-like mod for 3D
	DFT Exchange Formats	imec	IEEE	To enable Scan/JTAG across tiers
Standard		**Driver**	**Keeper**	
Materials Material compatibility	Metallurgy pairs			Compatible metallurgies
	Max dT safe operating area	SEMATECH	SEMATECH	SoA spec for compatible metallurgies
	Reliability SoA			Rel SoA spec for compatible metallurgies
QA Incoming specs	Metrology (e.g., warpage)	SEMATECH		How to measure warpage – not numbers
	Die/wafer QA metrics	SEMI	JEDEC	How to measure chip, balls, planarity…
Flow Handling specs	Shipping carrier specs – Bonded wafer pair	SEMATECH	SEMI	Shape size, etc., required for machines
	In-assembly ESD	OSAT	ANSI/ESDA	Requirement & verification
Test	KGD/pre-bond test	imec	IEEE	Methodology, flow, sacrificial pads
	Probe cards	imec		Prob pads formats, etc.

Figure 2. Standards Landscape *(Courtesy: Nick Yu, Qualcomm – SEMICON Taiwan, September 2010)*

Standardization is also driven by the needs of the end-user. Companies assembling chipsets for use in cell phones, PCs, tablets and other applications typically source the chips from multiple suppliers. For a cost-effective stacked solution, similar chips from different suppliers must be interchangeable. This makes interface standards critical since their absence would curtail high-volume production, relegating the technology to niche applications.

A third factor comes from the promise of 3D stacking. If the interfaces between levels or tiers are fully standardized, these different levels can be mixed and matched, allowing end-users to customize the functionality and performance of their products with an expeditious time to market. This would allow new products to be rapidly deployed at considerably lower development costs with the potential that these costs can be recovered in a timely manner. This is critical at a time when the industry is facing long development times for complex products amid spiraling technology costs, making 3D an industry game changer.

- 12 companies surveyed Aug-Sep 2010: IDMs, foundries, fabless, OSATs
- High-density via-mid applications including interposers, heterogeneous stacking, logic on logic, memory on memory; 2011-2014 time frame
- Addresses all aspects of via-mid: wafer processing, assembly, reliability, inspection/metrology, design, test
- Highest priorities for heterogeneous stacking (e.g., wide IO DRAM) shown below

Gaps in Standards and Specifications

- EDA Exchange Formats
  Partitioning and floor planning; logic verification; power/signal integrity analysis; thermal analysis flow; stress analysis flow; physical verification; timing analysis
- Reliability
  Reliability test methods
- Test
  DFT test access architecture
- Inspection/metrology
  TSV voids, defect mapping, microbump inspection and coplanarity
- Chip Interface
  Stackable memory pin assignment; stackable memory physical pinout
- TSV
  Keep-out area, fill materials, dimensions
- Thin wafer handling
  Universal thin wafer carrier

Technology Development and Cost Reduction

- Reliability
  Criteria; test methods; ESD
- Temporary bond/debond cost reduction
  Materials and release mechanisms cost reduction; equipment cost reduction
- TSV
  Keep-out distance/area
- Microbumping and bonding
  Pad metallurgy and layer thickness; bump metallurgy
- Inspection/metrology
  Microbump inspection and coplanarity; TSV voids; BWP voids
- Test
  Probing microbumps cost reduction

Figure 3. SEMATECH Survey on Gaps in the Via-Mid Ecosystem

Specificities of Standardization

A key differentiator of 3D from conventional semiconductor technology is that 3D technology impacts the entire semiconductor landscape from silicon wafers through design, fabrication, assembly and test. As a result, standards addressing each of these areas must be revisited. In addition, due to the novelty of TSV technology, completely new standards may also be needed to provide the requisite "comfort factor" for high-volume manufacturing and ensure interoperability.

A comprehensive treatment of the issues involved in standardization has been provided by Nick Yu.[4] As shown in Figure 2, compatibility among chips is needed for layout, modeling, design databases, materials, incoming specs, handling specs, quality assurance specs, and test. Several of the entities responsible for creating these standards, such as JEDEC, SEMI, ANSI/ESDA, IEEE and SI2, have recently issued press releases on standardization. Figure 2 also lists some possible champions or "drivers" for these standards activities. As can be seen, each organization is responsible for very specific areas. To ensure that the right standards are in place in time for high-volume front-runner products, all these organizations must work together in a coordinated fashion.

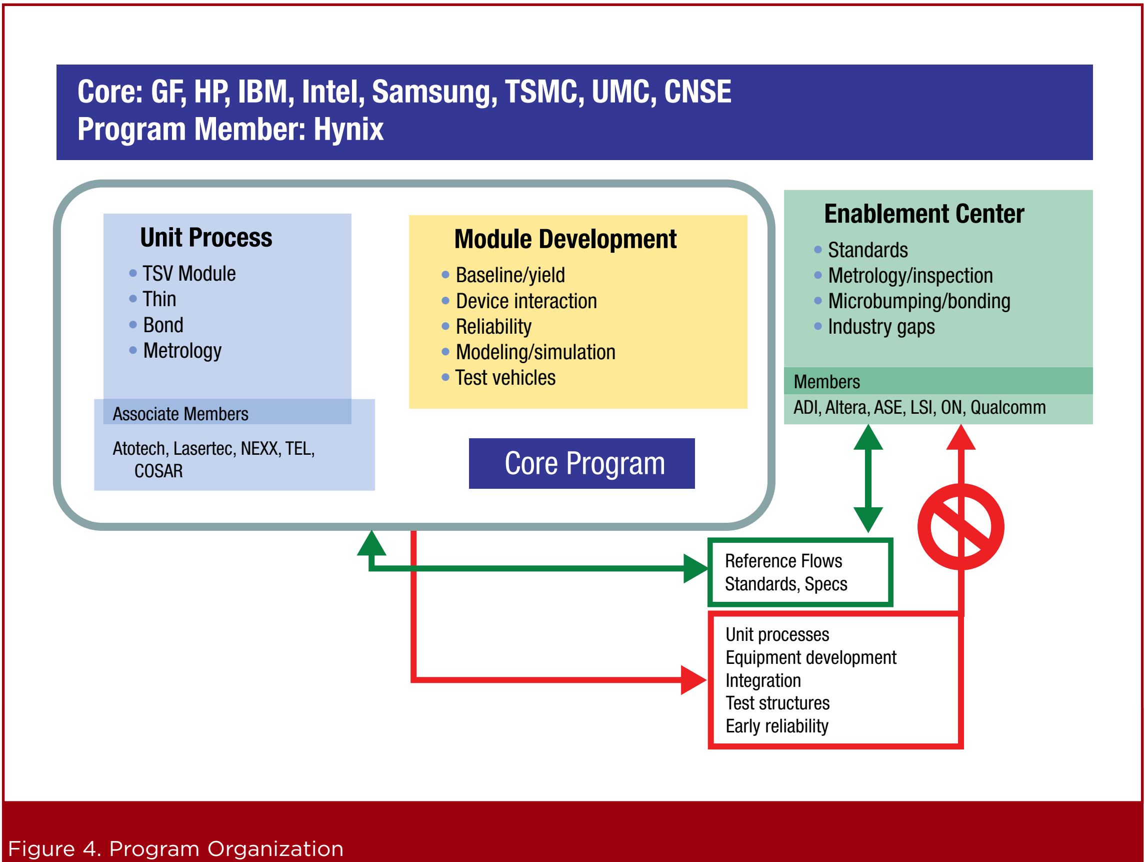

Figure 4. Program Organization

Figure 3 shows the results of a SEMATECH survey of the standards landscape.[5] An important conclusion was that the number of current standards organizations appeared adequate; new ones should not have to be created. Certain topics also had enough background material and data to be standardized: EDA exchange formats, reliability, test, inspection/metrology, chip interface, TSV, and thin wafer handling. Other areas, however, still require technology development before initial specifications can be decided, which in turn will generate the data to develop standards: reliability, temporary bond/debond cost reduction, TSV, microbumping and bonding, inspection/metrology and test.

Driving 3D Standards at SEMATECH

Under the aegis of the Semiconductor Industry Association, SEMATECH in partnership with the Semiconductor Research Corporation (SRC) launched the 3D Enablement Center (3D EC). The mission of the 3D EC is to ensure industrywide readiness for cost-effective TSV-based 3D-stacked IC solutions. As shown in

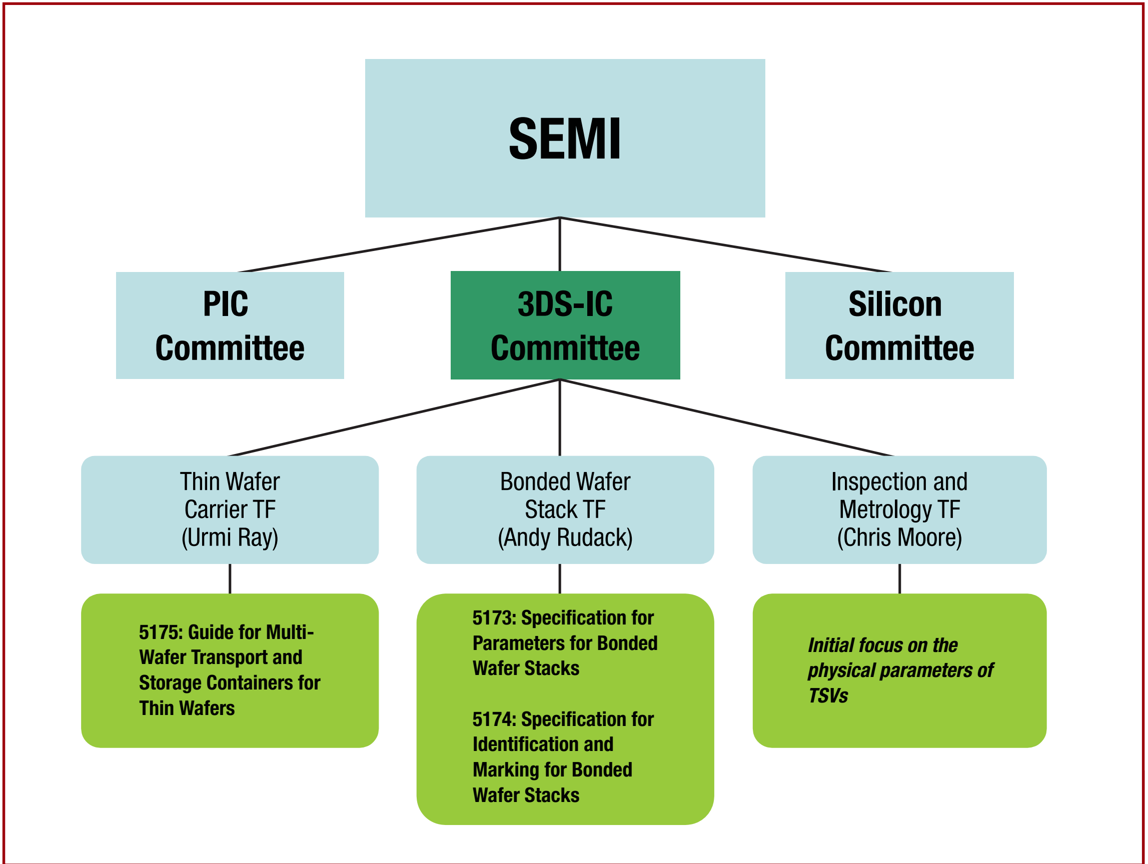

Figure 5. SEMI 3D Standards Activities

Figure 4, the members of the 3D EC are Analog Devices Inc, Altera, ASE, LSI, On Semiconductor and Qualcomm, in addition to SEMATECH's regular members (GLOBALFOUNDRIES, HP, Hynix, IBM, Intel, Samsung, TSMC, UMC and the College of Nanoscale Science and Engineering). As demonstrated by the technical and geographical diversity of the companies, 3D EC membership is open to all semiconductor companies.

While intended to jump-start the industry's 3D standardization efforts and leverage the combined member input and SEMATECH and SRC R&D capabilities, the 3D EC aims to develop pathfinding and EDA tools with complex "productlike" test vehicles envisioned in future phases.

Consisting of assignees from member companies as well as SEMATECH direct hires, two active working groups on standards/metrology and reference flows collect member input on topics including the 3D standards landscape, technology- and specifications-supporting standards, inspection and metrology (for TSV and bond voids, wafer thickness, and warpage), microbumping and bonding specifications, and near-term university research (managed by the SRC). SEMATECH then channels this input into the appropriate standards body. For example, close cooperation with SEMI has resulted in the formation of the 3D SIC committee with three task forces: thin wafer carriers, bonded wafer stacks and inspection/metrology. The organization, together with the task force leaders and the appropriate standards, is shown in Figure 5.

Summary and Conclusions

3D TSV technology represents a significant revolution in the industry. Understanding and addressing the changes and gaps in the ecosystem will be aided considerably by the availability of credible reference flows and accompanying standards. SEMATECH is working with its members to address standardization and ensure the readiness of the infrastructure for high-volume manufacturing of the first products.

References

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About the Author

Sitaram R. Arkalgud

Dr. Sitaram R. Arkalgud is director of SEMATECH's Interconnect Division, which focuses on new interconnect technologies for tomorrow's advanced computer chips. He has over 18 years of R&D and manufacturing experience in areas within the chip industry. Arkalgud has authored over 25 publications and holds 14 U.S. patents. He has a doctorate and master's degree in materials engineering from Rensselaer Polytechnic Institute in Troy, N.Y., and a B.S. in metallurgical engineering from Karnataka Regional Engineering College, Surathkal, India. ■