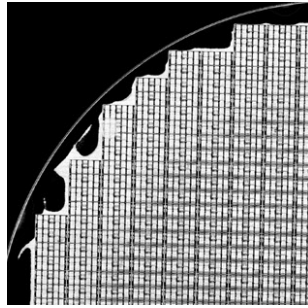


Stacking the Chips



SEMATECH's 3D Interconnect Program



SEMATECH: The world's catalyst for accelerating the commercialization of technology innovations into manufacturing solutions.

The next technology revolution won't come from a lab. It won't be driven by a single company. It will come from effective collaboration and smart partnerships that translate today's innovative ideas into the products of tomorrow.

At SEMATECH the world comes together to speed the commercialization of technology innovation, from research and development to manufacturing.



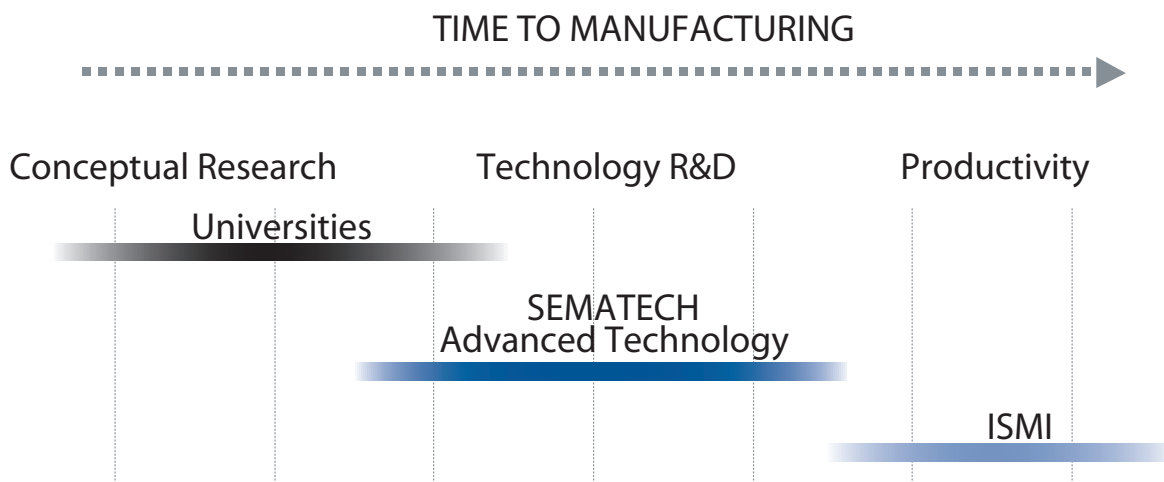
Lithography, Interconnect, Materials and Emerging Technology

SEMATECH conducts state-of-the-art research on the technical challenges and costs associated with developing new materials, processes, and equipment for semiconductor manufacturing. Advanced technology programs focus on immersion and EUV lithography, low-k materials and 3D architecture, and high-k materials and next generation transistors.

Manufacturing Productivity

International SEMATECH Manufacturing Initiative (ISMI) operates six programs encompassing a total of 30 projects—all focused on increasing productivity and decreasing costs for our members. They include:

- ESH Technology Center
- Continuous Improvement
- ISMI Councils
- Metrology
- Next Generation Factory
- 450 mm Transition



At SEMATECH, some of the biggest names in the semiconductor business come together to leverage resources, increase productivity, and lower costs.

We have a proven history of making sure member companies can afford to stay on the productivity curve.

We reduce cost and risk

We are a companion to members' R&D processes and help develop aspects of technology more quickly and economically than members could on their own by reducing options to the most workable solutions.

Rather than each member company funding solutions individually, we enable members, using what they learn at SEMATECH, to spend more resources on developing their own competitive advantage.

We deliver exclusive benefits to our members

First-to-market solutions – Members get full and detailed, actionable data.

Cost avoidance – Members avoid spending the full R&D costs of ultimately unworkable solutions and lower their learning curve for new processes.

Inside track – Members receive early evaluation of new materials and technologies without contamination and equipment risk in their fabs.

We are flexible both in memberships and programs

Members help shape the programs.

We offer a variety of ways to work with us.

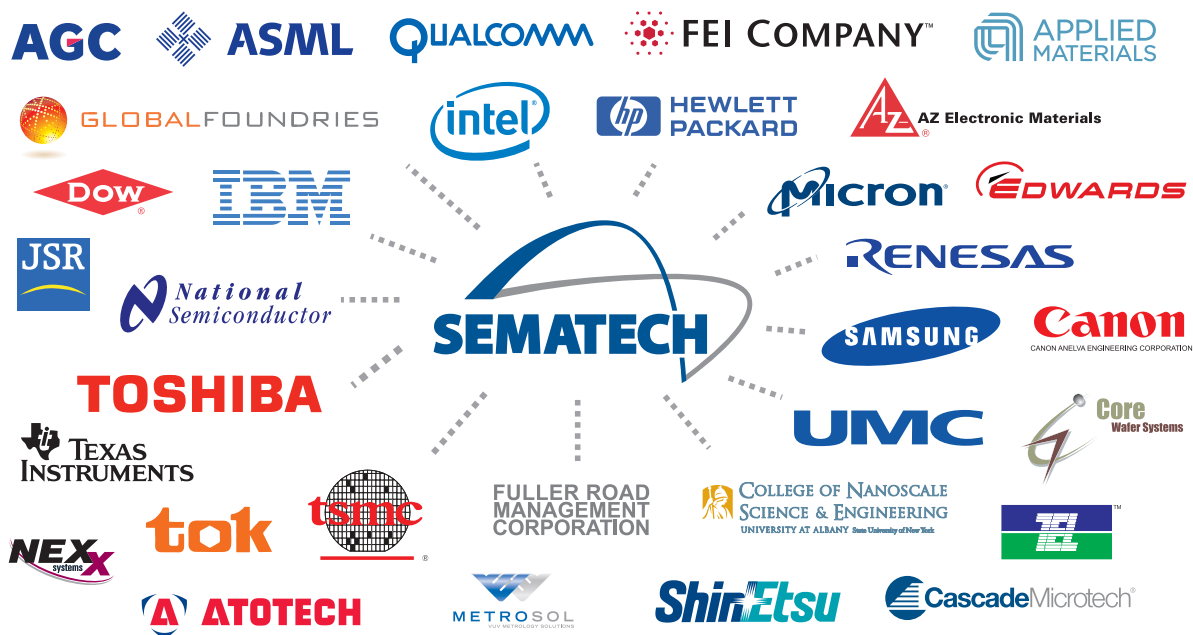
We span the timeline from research to development to manufacturing.

We have a proven record of success

We have nearly 20 years of experience in moving the industry forward.

SEMATECH is a well-cited and long-standing example of a successful public/private partnership.

During a period of rising industry uncertainty, it becomes increasingly important to spend R&D money wisely. SEMATECH believes that building strategic collaborations to avoid unnecessary costs while staying close to emerging innovations is the best way to keep your company moving forward as the industry creates the next technology revolution.



SEMATECH's 3D Interconnect Program

Using deep through-silicon vias (TSVs) to electrically connect a stack of chips, 3D interconnect technology bonds semiconductor wafers and die to produce multilevel chips with an optimum combination of cost, functionality, performance, and power consumption. When proven feasible for volume manufacturing, 3D will provide a path toward integrating diverse CMOS technologies with each other and CMOS chips with emerging technologies such as MEMS and bio-chips in a cost-effective manner.

SEMATECH's 3D Program is the follow-on to almost ten years of work at SEMATECH to develop robust copper/low-k interconnect technology. As these classical CMOS solutions are now being actively implemented in our member fabs, we have moved on to the next-generation interconnect solution—TSVs.

The advantages of 3D-TSV over the alternatives

By combining the performance and power of system-on-chip (SoC) with the functionality and time-to-market advantages of system-in-package (SiP), TSV offers the best of both for achieving very high densities for memory and logic. Its advantages over SoC and SiP include the following:

- Greater density for the same footprint
- More functionality
- Higher performance
- Lower power consumption
- Lower cost
- More manufacturing flexibility
- Faster time to market

The right partners delivering the right solution

SEMATECH's ability to bring together the right partners from across the entire industry—chipmakers, equipment and materials suppliers, and assembly and packaging service companies—is crucial to making 3D-TSVs the right solution for high volume manufacturing (HVM). Furthermore, by using strengths developed over our 20-year history in organization, technology assessment, and benchmarking, we have built our program to solve the challenges of 3D-TSV by:

- Driving industry consensus on integration approaches, process architectures, and tool sets
- Increasing knowledge of process flow costs and product dependencies
- Developing mature specific unit processes
- Creating a roadmap and driving for standards

SEMATECH's successful track record in preparing new technologies for manufacturing—including 300 mm wafers, 193 nm immersion, and high-k and low-k materials—will give 3D program members a clear advantage in overcoming the challenges and accessing the advantages of 3D-TSVs. Membership in SEMATECH's 3D Program will:

- Reduce cost and risk for members
- Provide members with early access to this breakthrough technology
- Allow members to formulate and drive standards
- Give members cost-effective, manufacturable solutions

2010 Project Goals

3D Equipment Characterization and Development:

The complete equipment set necessary for via-mid TSV technology will be acquired, installed, and qualified. Characterization and development will include both die/wafer processing as well as associated metrology, including a state-of-the-art wafer bonder from EVG capable of both Cu-Cu thermocompression and fusion bonding, a wafer backgrind tool from Okamoto, a wet hood for chemical thinning and cleaning, and a TSV depth metrology tool from Lasertec. Selected tools will undergo equipment development and hardening to ensure a robust equipment set for 3D TSV technology.

A via-middle die-to-wafer (DtW) integration will be supported with reliable 5x50 micron TSVs and Cu-Cu bonding. The program will deliver optimized processes for the TSV module (5x50 micron TSV RIE, liner/barrier/seed, Cu plating and Cu CMP), handle wafer bonding, wafer thinning, TSV exposure, Cu-Cu thermocompression bonding, and backside metallization.

The 3D metrology supplier chain will be cultivated along with a comprehensive assessment of metrology challenges and techniques. Work will include evaluating different metrology techniques for in-line TSV depth and profile measurements, as well as evaluating the suitability of different metrology techniques (SAM, IR) for implementation in HVM to assess bond quality.

Access to the 3D equipment infrastructure at SEMATECH/CNSE will support the early evaluation and implementation of this technology at our member companies.

3D TSV Module Development

A robust 5x50 micron TSV module will be delivered to enable the characterization and development of the equipment and processes. The yield and reliability of TSVs as a function of processing conditions will also be characterized.

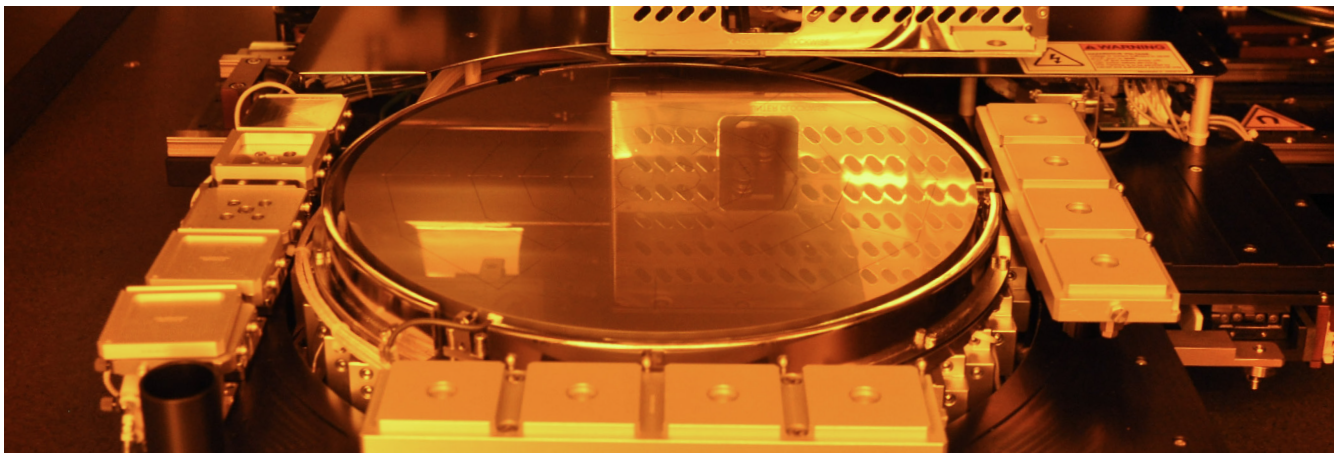
Thermo-mechanical modeling will be developed to characterize stress near TSVs and the dependence of stress on TSV diameter, pitch, A/R, shape, configuration, and thermal histories using the best known method (BKM). Micro-Raman spectroscopy will be evaluated in conjunction with finite element modeling in support of the DtW 5 x 50 μm reference flow.

3D DtW Module Development

A reliable DtW integration incorporating TSVs to enable the characterization and development of the equipment and processes will be demonstrated.

Industrywide Consensus Building

Members will participate in standards and roadmapping organizations and activities, and SEMATECH workshops will be organized around critical 3D elements such as metrology, stress management, and standards to drive industry consensus on 3D.



SEMATECH's 3D Interconnect Program

2008 Technical Milestones

- Installation and qualification of a TEL TSV RIE tool, which is now demonstrating 1 micron wide vias, has enabled state-of-the-art development in TSV metallization, fill, and CMP.
- A scanning acoustic microscope (SAM) was acquired, and orders were placed for an infrared microscope and Cu plater, advancing SEMATECH's capability to demonstrate working TSV chains and bonded wafers in-house at CNSE. Other state-of-the-art 3D tool acquisitions are in progress to enable complete development and exploratory capability at CNSE.
- Two materials (HT 10.10 and bibenzyl) were evaluated, and a report on the findings was delivered to the members. These two materials were the first to be studied in a comprehensive materials evaluation and characterization program for temporary and permanent bond materials.
- The manufacturability of the in-house wafer aligner/bonder was evaluated and its alignment accuracy, manufacturability, and cost of ownership were studied.
- In partnership with CNSE, comprehensive TSV test structures were laid out for both wafer-to-wafer and die-to-wafer integration schemes. This test vehicle will allow the impact of 3D processes (TSV formation, bonding, thinning, etc.) on transistors and CMOS circuitry to be studied.
- SEMATECH took a lead role in driving a high density TSV roadmap for the *International Technology Roadmap for Semiconductors* (ITRS) during 2007/2008.

2009 Technical Milestones

- In cooperation with CNSE and Binghamton University of the State University of New York (SUNY), we identified the metrology techniques and target metrics for evaluating bond material performance. Eight materials were characterized; one temporary bond material meeting requirements for the tack bond process was delivered.
- The program installed and qualified the SET FC300 die bonder, Olympus infrared (IR) microscope, and the Sonix SAM, completing all in just days following the tools' arrival.
- 3D achieved yielding via chain results for both wafer-to-wafer and die-to-wafer integration, with submicron alignment accuracy.
- Working jointly with CNSE and member companies, we completed a thorough evaluation of existing leading-edge wafer aligner/bonder capabilities.
- 3D demonstrated world-class TSV reactive ion etch (RIE) results (1 μm wide and 20 μm deep TSVs) using a non-Bosch process. We also identified a tool with the capability to measure the depths of 1 μm wide TSVs.
- Startup reports were completed for the Tokyo Electron (TEL) TSV RIE tool, as well as the Sonix SAM, the Olympus IR microscope, and the SET FC300 die bonder. Cost-of-ownership estimates were completed for these tools and the EVG 540 aligner/bonder (manual). Manufacturability assessments were completed for the TSV RIE tool, the EVG 540 aligner/bonder, the SAM, and the IR microscope.
- The program successfully processed bonded, edge-trimmed, and thinned wafers through backside back-end-of-line (BEOL) metallization, demonstrating the manufacturability of bonded wafer processing in front-end fabs.
- Finally, we worked with the ITRS to better define the use of TSVs. The 2009 Interconnect chapter now contains a hierarchy of TSV levels, allowing for a better understanding of the types of 3D interconnects.

Publications of Interest

IR Microscopy as an early indicator for electrical yield in 3D Integration

Author: Andy Rudack

Publication: SPIE, March 2010 and Wafer and Device Packaging and Interconnect (WDPI), April 2010

Manufacturable 300mm Wafer Thinning for 3D Interconnect Applications

Author: Jamal Qureshi

Publication: Materials Research Society, March 2010

Backside Infrared Interferometric Patterned Wafer Thickness Sensing for Applications in Through-Silicon-Via (TSV) Etch Metrology

Author: Weng Hong Teh

Publication: Applied Physics Letters, January 2010

A route towards production-worthy 5um x 25um and 1 um x 20um non-Bosch through-silicon-via (TSV) etch, TSV metrology and TSV integration

Author: Weng Hong Teh

Publication: IEEE 3DIC Conference, May 2009

300 mm wafer-scale production-worthy anisotropic through-silicon-via etch using magnetically-enhanced capacitively-coupled plasma for 3D integration

Author: Weng Hong Teh

Publication: IEEE Trans. Semicon Manufacturing, April 2009

Magnetically-enhanced capacitively coupled plasma etching for 300 mm wafer-scale fabrication of CU through-silicon-vias for 3D logic integration

Author: Weng Hong Teh

Publication: IITC 2009, January 2009

Exploring Memory-on-Logic 3D IC Technology for DSP and Secure Computing

Author: Larry Smith

Publication: IEEE Design and Test of Computers, January 2009



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